IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):

Debanjan Mukherjee; Jishnu Bhattacharjee; Qian Yu; & Abhijit Phanse

Assignee:

Scintera Networks, Inc.

Title:

Analog Delay Elements

Serial No.:

10/724,443

Filing Date:

November 26, 2003

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Examiner: Docket No.: Ngo, Chuong D. M-15287 US

Group Art Unit: 2193

Confirmation No.:

Irvine, California October 15, 2007

Mail Stop Issue Fee Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit four (4) sheets of formal drawings, consisting of Figures 1-6, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (949) 752-7040.

Certificate of Transmission

I hereby certify that this correspondence is being sent via EFS Web to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date stated below.

FLECTRONICALLY FILED

October 15, 2007

Respectfully submitted,

Greg & Michelson

Greg J. Michelson Attorney for Applicants Reg. No. 44,940

LAW OFFICES OF REPHERSON KWOK CHEN

SUITE 210 IRVINE, CA 92612 (949) 752-7040 PAX (949) 752-7049